Advanced characterization of gate oxides for 4H-SiC MOSFETs

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4H-SiC MOSFETs are already commercially available, the SiC community is still devoted to optimization of several processing step and to the comprehension of the threshold voltage (V_{th}) instability phenomena [i,ii]. These latter are due to electron trapping at near-interfacial oxide traps (NIOTs) that extend spatially into the gate oxide from the SiC interface. Near-equilibrium gate-capacitance [iii] and gate- [iv] and drain-current transient measurements allowed to get insight on the impact of NIOTs on the device characteristics and V_{th} stability. In particular, transient gate-capacitance and gate-current measurements allowed us to estimate firstly the position (about 1 nm from the SiC interface) and secondly to quantify the amount (2×10^{11} cm^{-2}) of the NIOTs. Furthermore, the nature of this NIOTs has been discussed on the basis of the interface microstructure [v]. Finally, results on the process development and characterization of novel gate oxide with high-permittivity will be presented [vi].

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