The Quickplay High Level Synthesis flow to target FPGA-based accelerators

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After shortly reviewing what an FPGA is and the benefits achievable through the adoption of FPGA devices, the High-Level Synthesis tool QuickPlay is presented. QuickPlay is a design flow which allows to completely abstract from the HW details of the FPGA, as the configuration bitstream is achieved through the compilation of a design represented through the connection of several communicating computing kernels, each represented by means of a C function communicating through dedicated I/O streams: the underlying computing model is the Kahn Process Network. QuickCompiler, the HLS engine of QuickPlay, translates each C kernel into an efficient HW architecture; all the connections between the kernels, the instantiation of the IPs for I/O communications (PCIe, DDR controllers) as well as clock and reset distribution and all the other low-level details are managed by QuickPlay in a transparent way. QuickPlay is able to address FPGA families produced both by Intel and Xilinx, allowing an easy migration across different technologies.